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10/811,407	03/26/2004	Dale W. Schroeder	10030930-1	3279

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EXAMINER	
SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,407	SCHROEDER, DALE W.	
	Examiner	Art Unit	
	Grant D. Sitta	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-32* is/are pending in the application.

4a) Of the above claim(s) *2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/15/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 30 is objected to because of the following informalities: "loading the data into one set the light...". It is believed "loading the data into one set of the light..." Appropriate correction is required.

2. Claim 22 is objected to because of the following informalities: It contains two sentences. Examiner believes applicant intended the second sentence to be claim 23. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 ,4 ,9, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Muir et al (3,374,463) hereinafter Muir.

3. In regards to claim 1, Muir teaches circuit elements arranged in an array of rows (fig. 2 A-E) and columns (fig. 2 15-0), said circuit elements being alterable (col. 7, lines 55-75) in response to data stored (fig. 1 "memory") therein and configured to shift data therebetween col. 7, lines 54-75 "steering" and col. 7, lines 1-5); and a strobe line (fig. 9 HL, HR, QR, and QL col. 24, lines 45-75) electrically coupled to ones of said circuit

elements constituting a set to provide thereto a strobe signal to cause said ones of said circuit elements in said set to shift data to non-adjacent (col. 8, lines 1-4 "diagonal paths") ones of said circuit elements outside said set in an interleaving pattern (fig. 2 paths are interleaving, also see col. 7-8, lines 8-32), said set including row-adjacent and column-adjacent ones of said circuit elements (col. 8, lines 1-4 "diagonal paths").

4. In regards to claim 3, Muir teaches said strobe line is electrically coupled to ones of said circuit elements located in a first pair (col. 24-25, lines 45-4) of adjacent rows of the array to provide a first strobe signal (col. 24, lines 5-57 "control leads") to said ones of said circuit elements located in the first pair of adjacent rows (fig. 11 group A, B and C); and said electronic circuit additionally comprises an additional strobe line (fig. 11 XIA and XIB, and X2A and X2B) electrically coupled to ones of said circuit elements (fig. 11 AI8V, BI9V, etc.) located in a second pair of adjacent rows of the array to provide a second strobe signal to said ones of said circuit elements located in the second pair of adjacent rows col. 28-30, lines 73-68).

5. In regards to claim 4, Muir teaches wherein said first strobe signal is operable to shift data from (col. 24-25, lines 45-4) said ones of said circuit elements in the first pair of adjacent rows to said ones of said circuit elements in the second pair of adjacent rows (fig. 11 XIA, XIB,X2A, X2B, etc).

6. In regards to claim 9, Muir teaches a buffer connected to at least one end of the array to load the data into ones of said circuit elements (fig. 1 (101)).

7. In regards to claim 10, Muir teaches wherein said buffer is configured to load data into said ones of said circuit elements in at least a portion of at least two of the rows of the array (col. 6, lines 60-75) fig. 1 (101).

8. In regards to claim 11, Muir teaches wherein said buffer is configured to load data into said ones of said circuit elements in at least a portion of at least two of the columns of the array (col. 6, lines 60-75) fig. 1 (101). Examiner notes since the rows and the columns intersect, if data is loaded into the rows it is also loaded into the columns.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatake et al (2002/0092993) hereinafter Kanatake, in view of Bartholomew.

In regards to claim 21,Kanatake discloses the limitations of loading data (fig. 1 36 to 46) representing an image into light modulation elements (fig. 1 34,40,38); altering ones of the light modulation elements in response to the data loaded [0025-0028] therinto to transfer an instance of the image onto a substrate (fig. 1 (46) and altering ones of the light modulation elements (fig. 1 34,40,38) in response to the data shifted therinto to transfer another instance of the image onto the substrate [0025-0029],

Kanatake differs from the claimed invention in that Kanatake does not disclose a system and method for shifting the data between non-adjacent ones of the light modulation elements in an interleaving pattern.

However, Bartholomew teaches shifting (fig. 1 shift) the data between non-adjacent (fig. 1 45 to 51) ones of the light modulation elements in an interleaving pattern (fig. 2 24 and 31) (col. 4, lines 26-36). Examiner notes the connections are connected 75 diagonally and thus are not adjacent. Examiner also notes in fig. 1 the node connections between node 56 and the input bit 0 are interleaving.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Kanatake to include the use of non-adjacent elements and an interleaving pattern as taught by Bartholomew in order to reduce the time necessary to shift through the SLM.

3. In regards to claims 22 and presumptively claim "23",Kanatake teaches applying a voltage (fig. 1 36-52 and [0029]) in response to the data to the change optical characteristics of the light modulation elements [0029]. applying strobe signals to strobe

lines electrically coupled to respective ones of said light modulation elements ([0041 "The panel motor 55 is attached to the pixel panel 38 to move the pixel panel in two directions, represented by an x-arrow 132 and a y-arrow 134. The panel motor 55 may be a piezo electric device (PZT) capable of making very small and precise movements")

Bartholomew teaches to cause the data to be shifted between the non-adjacent ones of the light modulation elements (fig. 1 45 to 51).

4. In regards to claim 24, Bartholomew teaches utilizing a ripple clock to control the timing of said applying. (fig. 1 the input bit 0 is carried to the next stage)

5. In regards to claim 25, Kanatake teaches providing the light modulation elements arranged in an array of rows and columns (fig. 7 rows and columns [0045]).

6. In regards to claim 26, Kanatake teaches applying the strobe signals to respective sets of the light modulation elements, at least one of the sets comprising ones of the light modulation elements in at least a portion of at least two adjacent rows ([0050] "Pixel elements P11-P14 are on adjacent consecutive rows R1, R2, R3, R4 of column C1 of the pixel panel 38"); and

Bartholomew teaches shifting the data between the light modulation elements in non-adjacent rows (fig. 1 45 to 51).

7. In regards to claim 27, see the reason in claim 26

In regards to claim 28, Kanatake teaches applying the strobe signals to respective sets of the light modulation elements (fig. 1 (40)), at least one of the sets comprising ones of the light modulation elements (fig. 1 (40))

Bartholomew teaches at least two groups of orthogonally-adjacent (fig. 1 42 and 58) ones of said circuit elements, said at least two groups being positioned diagonally (fig. 2 24 and 31) in the array with respect to one another. (col. 1-2, lines 65-2).

8. In regards to claim 29, Kanatake teaches providing the light modulation elements arranged in an array of rows and columns (fig. 3 rows and columns); and
loading the data into the light modulation elements at one end of the array (fig. 1 (50)).

9. In regards to claims 30 and 31, Kanatake teaches loading the data into one set the light modulation elements in at least a portion of at least two rows of the array [0043-0045].

10. In regards to claim 32, Bartholomew teaches wherein said loading comprises loading data into a first section of the array in response to a first strobe signal (input bit 1) derived from a second strobe signal (input bit 0) used to shift data in a second section of the array (col. 4, lines 5-67).

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muir, in view of Kanatake.

12. In regards to claim 5, Muir discloses the limitations of claim 1,

Muir differs from the claimed invention in that Muir does not disclose wherein said strobe line is electrically coupled to ones of said light modulation circuit elements located in at least a portion of at least two adjacent columns of the array.

However, Kanatake teaches a system and method for wherein said strobe line is electrically coupled to ones of said light modulation circuit (fig. 1 40, 32, 48, 38, 39, 54, and 55) elements located in at least a portion of at least two adjacent columns of the array (fig. 7 [0043-0045]).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Muir to include the use of light modulation circuit as taught by Kanatake in order to use light modulation.

13. Claims 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muir, in view of Bartholomew.

14. In regards to claim 6, Muir discloses the limitations of claim 1,

Muir differs from the claimed invention in that Muir does not disclose wherein said strobe line is electrically coupled to at least two groups of orthogonally-adjacent ones of said circuit elements, said at least two groups being positioned diagonally in the

array with respect to one another.

However, Bartholomew teaches a system and method for wherein said strobe line is electrically coupled to at least two groups of orthogonally-adjacent (fig. 1 42 and 58) ones of said circuit elements, said at least two groups being positioned diagonally (fig. 2 24 and 31) in the array with respect to one another. (col. 1-2, lines 65-2).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Muir to include the use of orthogonally-adjacent elements as taught by Bartholomew in order to reduce the time necessary to shift through the elements.

15. In regards to claim 7, Bartholomew wherein said orthogonally-adjacent ones of said circuit elements are in at least two adjacent rows (fig. 1 (42 and 55)).

16. In regards to claim 8, Bartholomew wherein said orthogonally-adjacent ones of said circuit elements are in at least two adjacent columns (fig. 1 (42 and 55)). Examiner notes the difference between a row and a column is a matter of design choice.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muir

18. In regards to claim 12, Muir discloses the limitations of claim 9,

Muir differs from the claimed invention in that Muir does not explicitly disclose , wherein said buffer comprises buffer elements, each of said buffer elements loading data into a respective portion of the array, said strobe line being within a second portion

of the array and being connected to clock one of said buffer elements associated with a first portion of the array to load data into the first portion of the array.

However, Muir does teach wherein said buffer comprises buffer elements (fig. 1 (101), each of said buffer elements loading data into a respective portion of the array (fig.1 (100) and col. 6, lines 55-75), said strobe line being within a second portion of the array and being connected to clock (inherent) one of said buffer elements associated with a first portion of the array to load data into the first portion of the array (fig. 11 XIA, X2A, etc.).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Muir to include the use of clock as all circuitry needs some form of timing.

19. Claim 13, 14, 15, 16, 17, 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muir, in view of Kanatake.

20. In regards to claim 13, Muir discloses the limitations of claim 1,

Muir differs from the claimed invention in that Muir does not disclose wherein said circuit elements are light modulation elements, said light modulation elements including: memory elements configured to store the data and shift the data therebetween; and pixel controllers configured to alter the state of respective ones of said light modulation elements in response to the data stored in respective ones of the memory elements.

However, Kanatake teaches a system and method for disclose wherein said circuit elements are light modulation elements (fig. 1 36-46), said light modulation elements including: memory elements configured to store the data and shift the data therebetween; and pixel controllers (processor) configured to alter the state of respective ones of said light modulation elements in response to the data stored in respective ones of the memory elements. (claim 14, "a memory operable to store the pixel element; a pixel panel operable to receive the pixel element from the memory and project the pixel element onto a subject; a processor operable to rotate the pixel panel relative to the subject")

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Muir to include the use of light modulation circuit as taught by Kanatake in order to use light modulation.

21. In regards to claim 14, Kanatake and Muir teache wherein the memory elements include two groups of the memory elements, the pixel controllers (Kanatake claim 14) being controlled by the memory elements in an interleaving pattern (Muir fig. 2 paths are interleaving, also see col. 7-8, lines 8-32) between the two groups of memory elements (fig. 11 A and B) Examiner notes the groups can be grouped in odd and even or columns and rows.

22. In regards to claim 15, Kanatake and Muir teach wherein each of the memory elements further includes an output node electrically coupled to the respective pixel

controller and to an input node of a non-adjacent (Muir col. 8, lines 1-4 "diagonal paths") one of the memory elements [0043-0045].

23. In regards to claim 16, Kanatake teaches wherein said light modulation elements comprise liquid crystal material [0062 "LCD").

24. In regards to claim 17, Kanatake teaches the pixel controllers include pixel electrodes configured to receive the data stored in the respective memory elements (claim 14, "a memory operable to store the pixel element; a pixel panel operable to receive the pixel element from the memory and project the pixel element onto a subject; a processor operable to rotate the pixel panel relative to the subject"), and said light modulation elements (fig. 1 36-46) collectively comprise a common electrode configured to receive a common electrode signal for said light modulation elements (fig. 1 (50) [0026] says "line(s)" meaning one line or plural lines).

25. In regards to claim 18, Kanatake teaches said light modulation elements additionally include micromirrors ([0061] "microlenses"), and the pixel controllers comprise electromechanical devices (fig. 1 driver motor) configured to control the state of said respective ones of said micromirrors in response to the data stored in respective ones of said memory elements [0061 and 0029].

26. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muir.

27. In regards to claim 19, Muir discloses the limitations wherein said electronic circuit additionally comprises: additional strobe lines; and a shift register (col. 6 lines 5-25 fig. 1 110,100, and 104-106) electrically connected to said strobe lines to apply the strobe signals fig. 11, XIA, XIB, X2A, etc.).

Muir differs from the claimed invention in that Muir does not explicitly disclose applying to the strobe lines sequentially.
However, Muir implicitly contained within the reference. Examiner notes the bits are shifted out the right end (end) to the next node and are not reinserted at the left end (beginning) (col. 4, lines 58-75 of Muir).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Muir to include the use of applying to the strobe lines sequentially. as demonstrated from Muir in order to shift the data through the nodes as stated in (col. 4, lines 58-75 of Muir)

28. In regards to claim 20, Muir teaches wherein said shift register implements a ripple clock (fig. 1 (107) col. 6, lines 17-25). The accumulator may add two data words successively transmitted to it. And thus functions as a ripple clock.

29.

Response to Arguments

30. Applicant's arguments, see Applicant Arguments/Remarks made in an Amendment, filed 7/31/2007, with respect to the rejection(s) of claim(s) 1-32 under Bagley have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Muir 3,374,463, Bartholomew 5,696,803, and Kanatake 2002/0092993.

Conclusion

31. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 6/15/2007 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

October 9, 2007

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER